EE 435

Lecture 26

Data Converter Architectures

Data Converters

Types:

A/D (Analog to Digital)

Converts Analog Input to a Digital Output

D/A (Digital to Analog)

Converts a Digital Input to an Analog Output

A/D is the world's most widely used mixed-signal component

D/A is often included in a FB path of an A/D

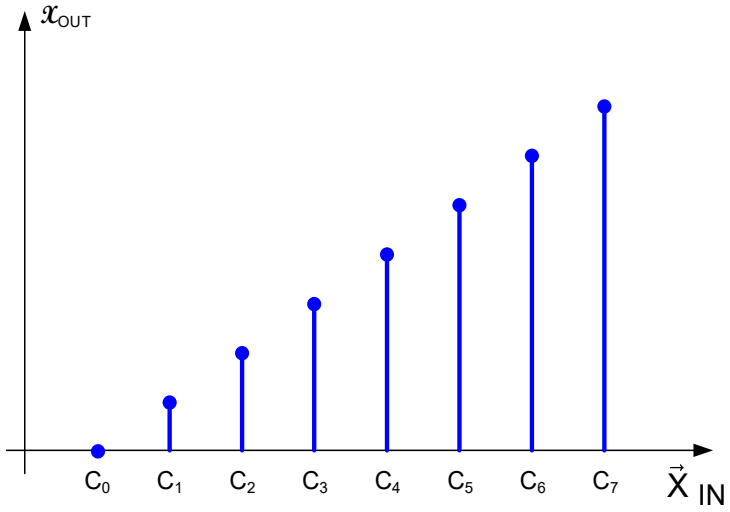
A/D and D/A fields will remain hot indefinitely

technology advances make data converter design more challenging

embedded applications

designs often very application dependent

D/A Converters



For this ideal DAC

$$x_{OUT} = X_{REF}\left(\frac{b_{n-1}}{2} + \frac{b_{n-2}}{4} + \frac{b_{n-3}}{8} + \ldots + \frac{b_1}{2^{n-1}} + \frac{b_0}{2^n}\right)$$

$$x_{OUT} = X_{REF}\sum_{j=1}^{n}\frac{b_{n-j}}{2^j}$$

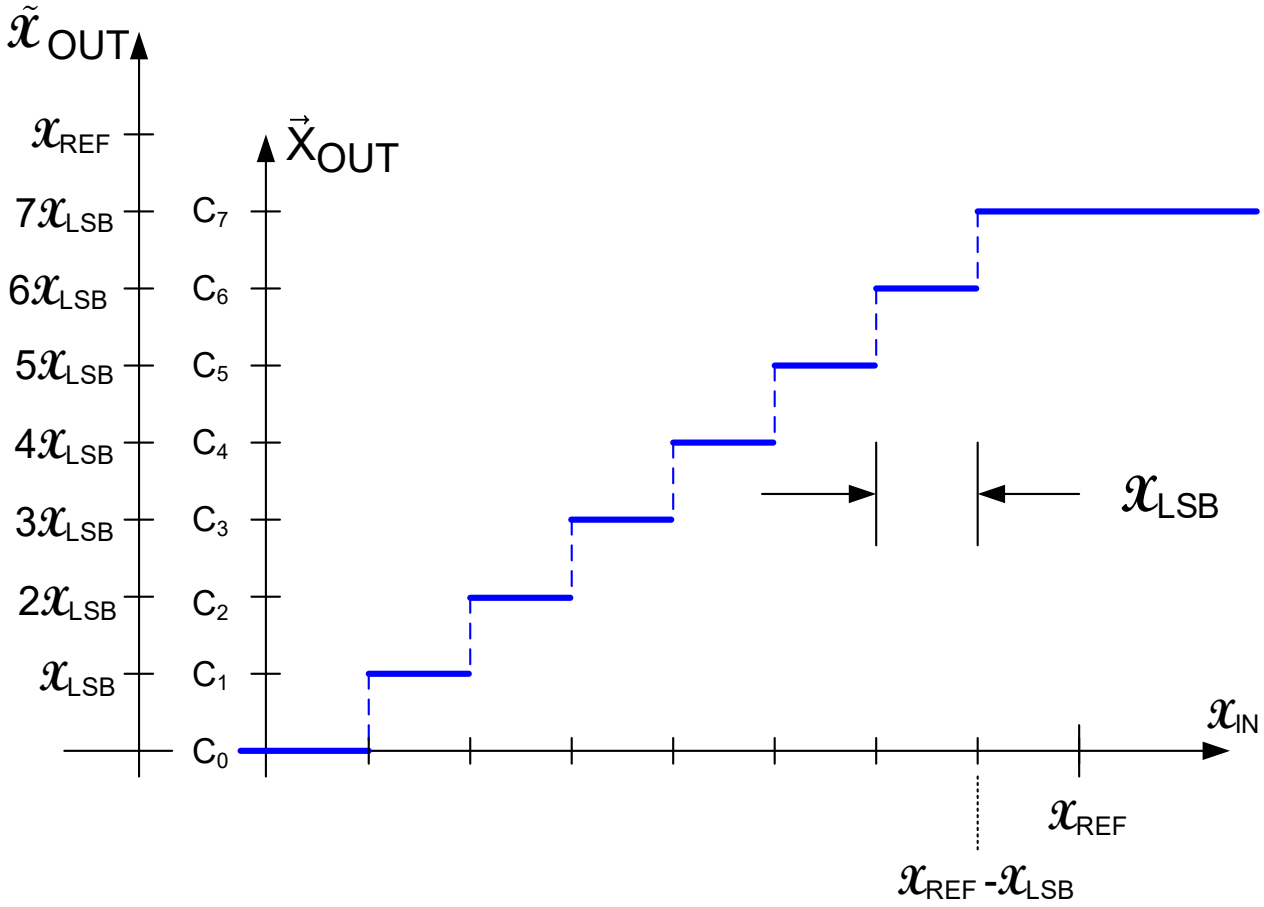
- Number of outputs gets very large for n large
- Spacing between outputs is $X_{REF}/2^n$ and gets very small for n large

A/D Converters

An Ideal ADC transfer characteristic (3-bits)

$\vec{X}_{OUT} = <d_{n-1}, d_{n-2}, \ldots d_0>$

$$x_{LSB} = \frac{x_{REF}}{2^n}$$

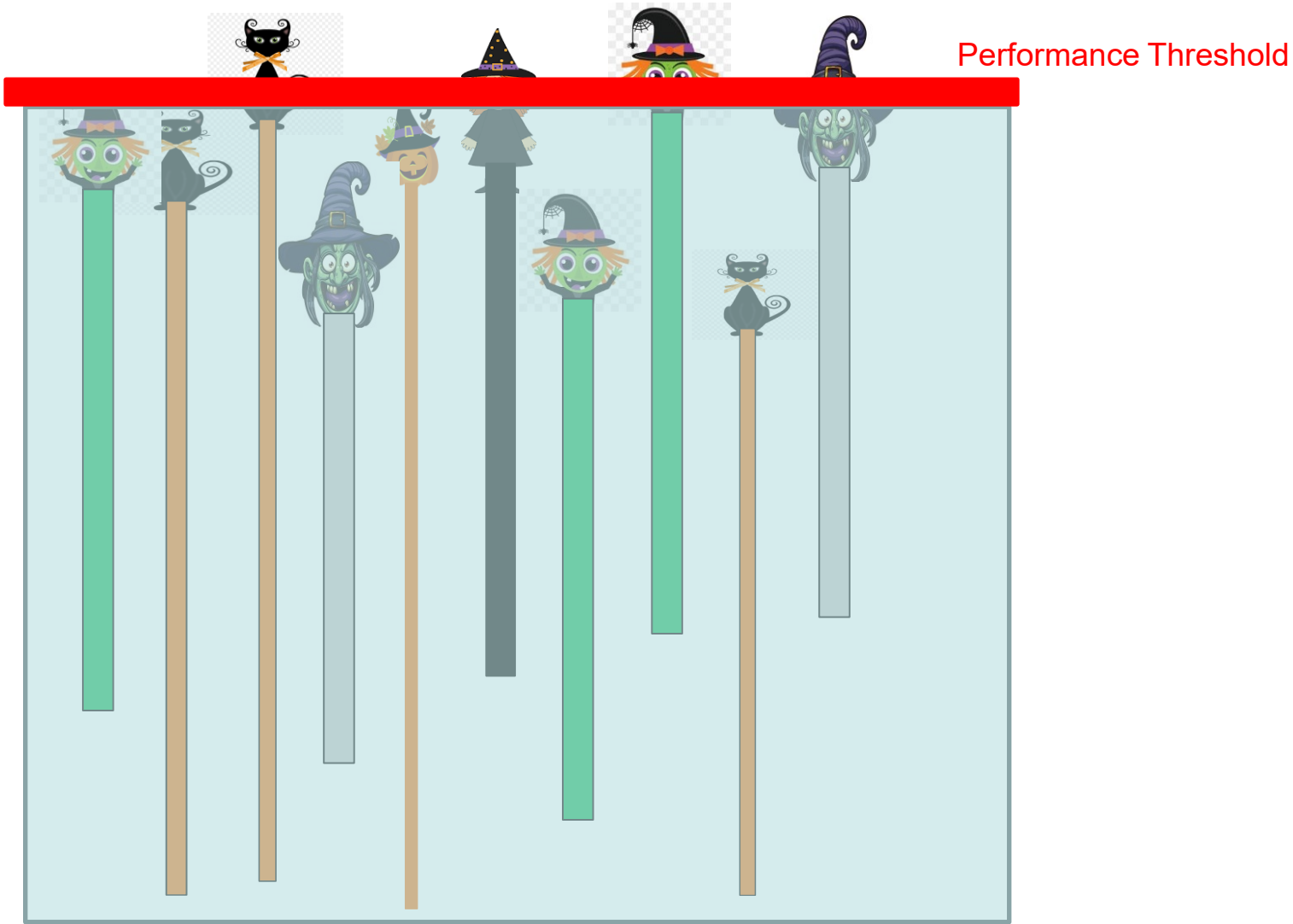


The second vertical axis, labeled $\tilde{x}_{OUT}$,is the interpreted value of $\vec{X}_{OUT}$

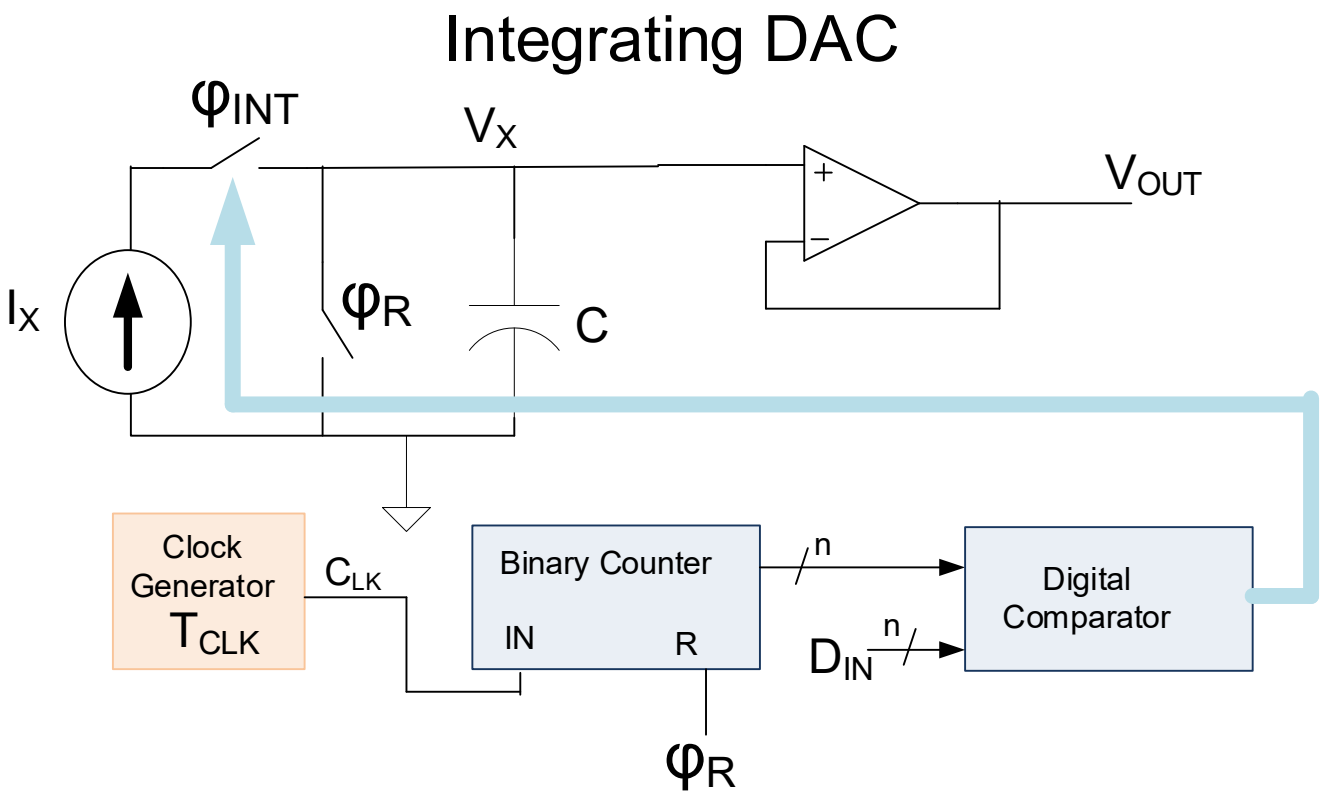
Data Converter Design Approach

Review from last lecture

Ultimately lowering (enhancing) performance threshold makes it difficult to further improve performance

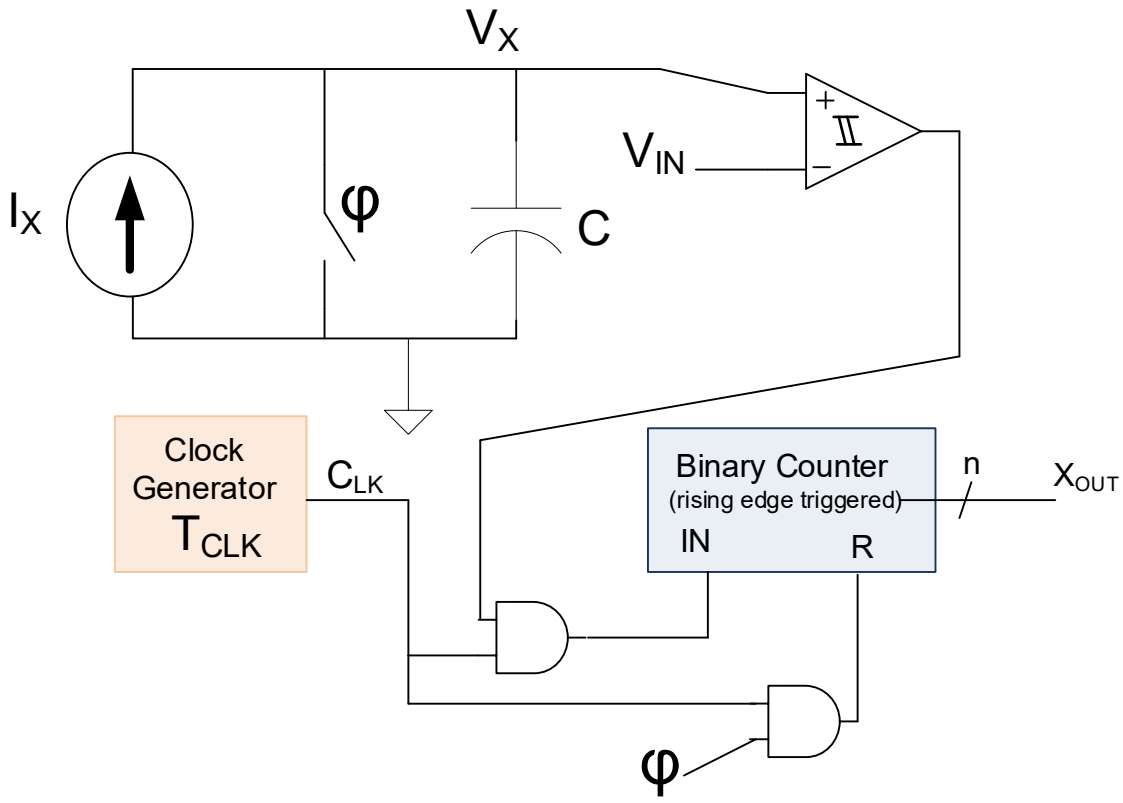


Very Simple DAC (discrete component)



Very Simple ADC (discrete component)

Single-Slope ADC



Data Converter Architectures

Strategy for discussing data converters

- Briefly look at some different data converter architectures
- Detailed discussion of performance parameters for data converters
- More detailed discussion of data converter architectures

Data Converter Architectures

Nyquist Rate

Flash
Charge Redistribution
Pipeline
Two-step and Multi-Step
Interpolating
Algorithmic/Cyclic
Successive Approximation (Register) SAR
Single Slope / Dual Slope
Subranging
Folded
Interleaved

Current Steering
R-string
Charge Redistribution
Algorithmic
R-2R (ladder)
Pipelined
Subranging

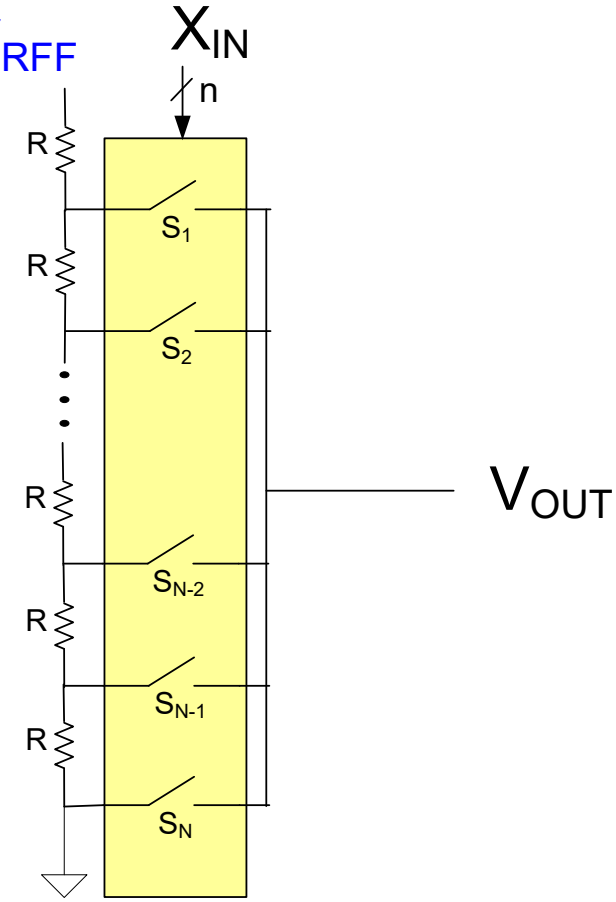
Over-Sampled (Delta-Sigma)

Discrete-time
First-order/Higher Order
Continuous-time

Discrete-time
First-order/Higher Order
Continuous-time

Data Converter Architectures

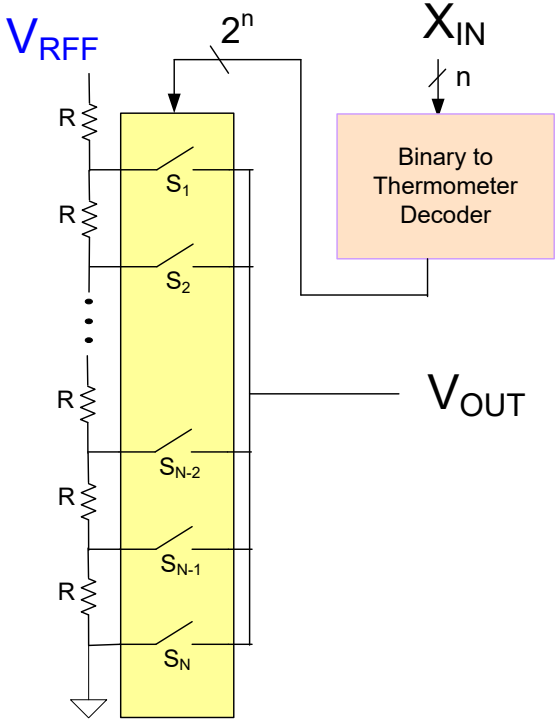
R-String



X_{IN} is decoded to close one switch

Data Converter Architectures

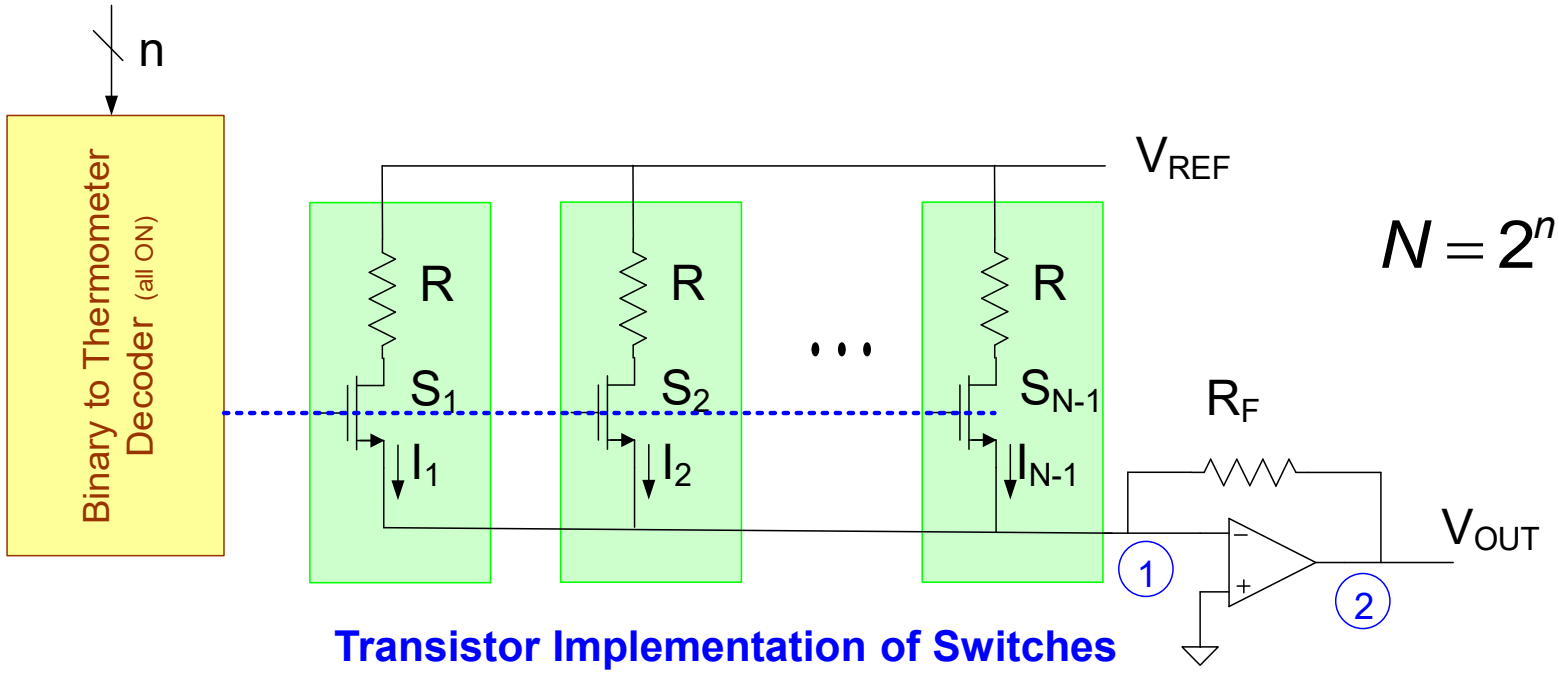
R-String DAC



Basic R-String DAC including Logic to Control Switches

Data Converter Architectures

Current Steering DAC

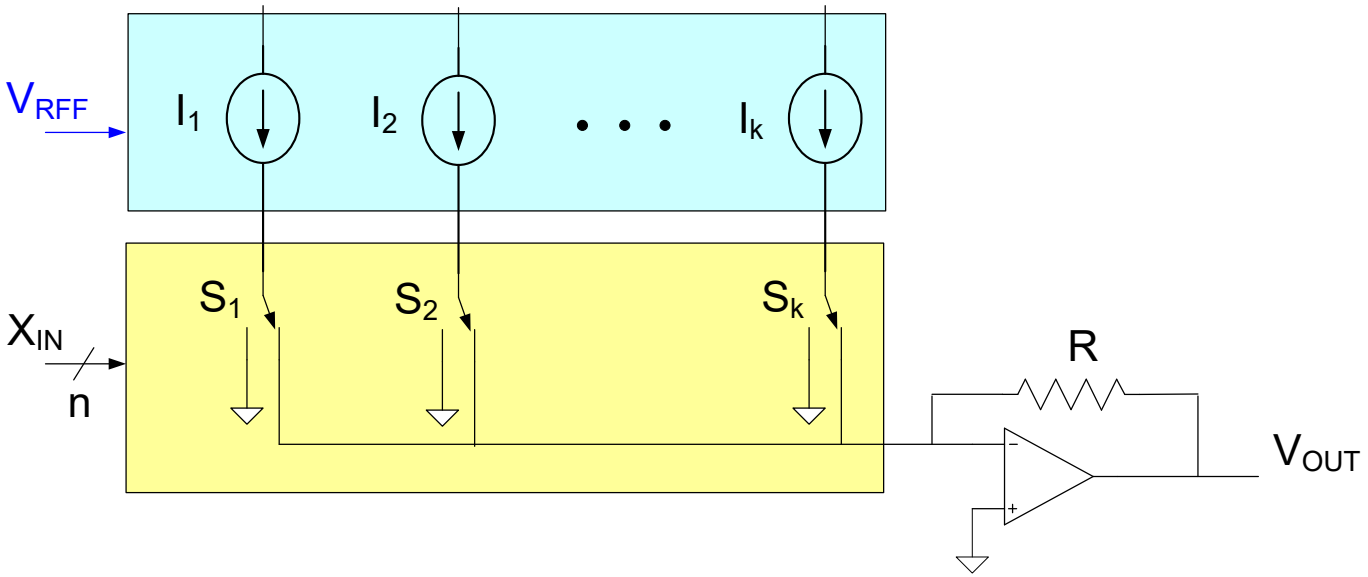


Transistor Implementation of Switches

Assume k switches are on 0<k<N-1 as determined by digital input code

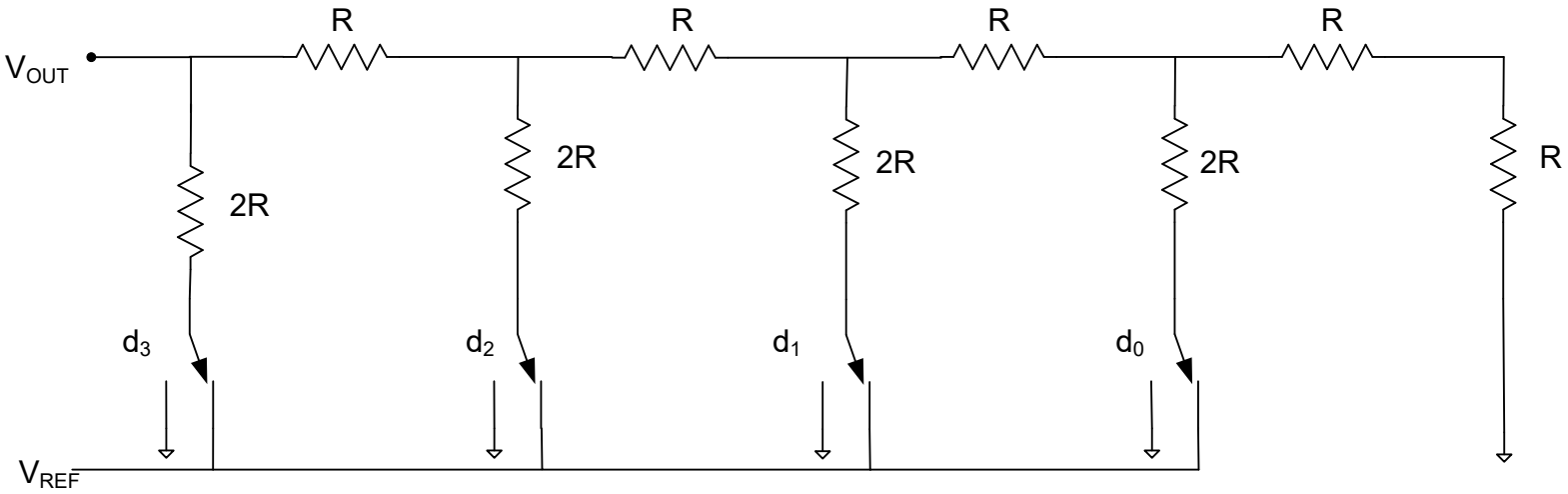
Data Converter Architectures

Current Steering



Data Converter Architectures

R-2R (4-bits)

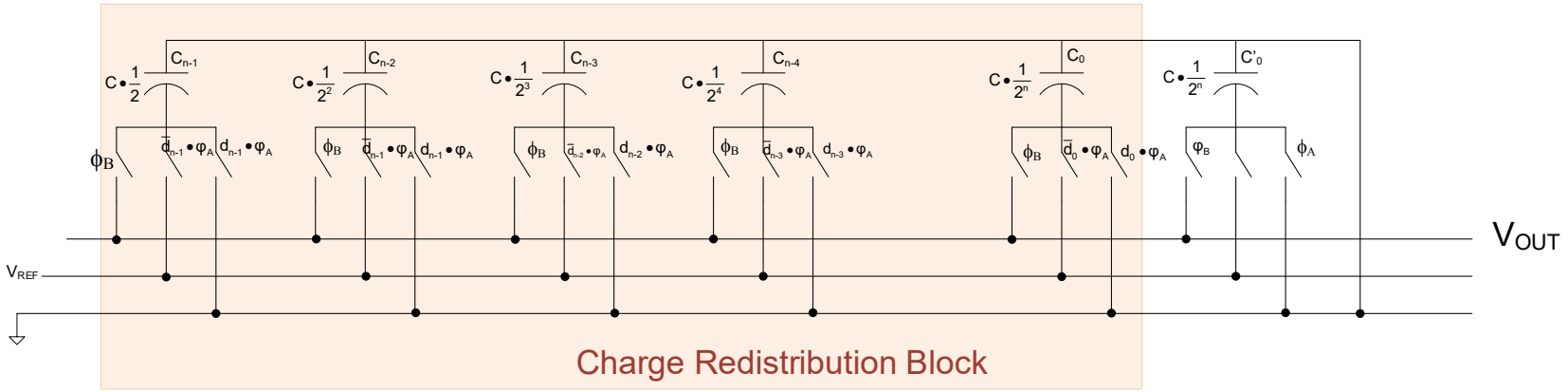


By superposition:

$$V_{OUT} = V_{REF} d_3 \cdot \frac{1}{2} + V_{REF} d_2 \cdot \frac{1}{4} + V_{REF} d_1 \cdot \frac{1}{8} + V_{REF} d_0 \cdot \frac{1}{16} = V_{REF} \sum_{k=0}^{3} \frac{d_k}{2^{4-k}} = V_{REF} \sum_{k=1}^{4} \frac{d_{4-k}}{2^k}$$

Data Converter Architectures

Charge Redistribution



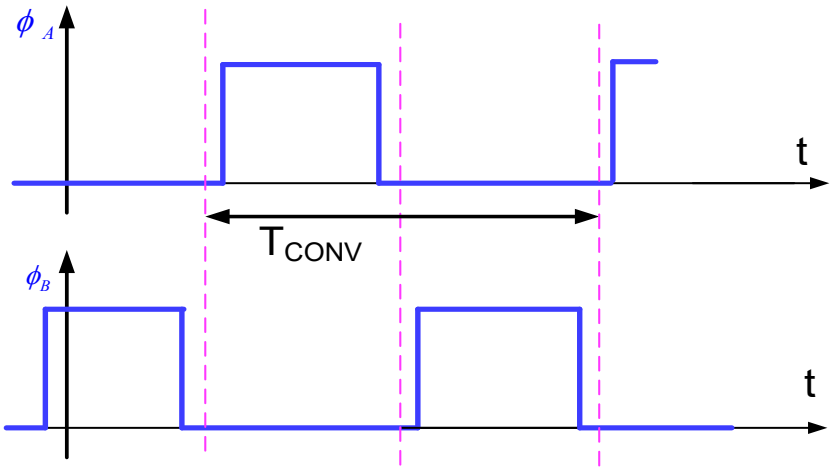
$$Q_{SET} = V_{REF} \sum_{i=0}^{n-1} d_i \frac{C}{2^{n-i}}$$

$$Q_{RDIS} = V_{OUT} \left(\sum_{i=0}^{n-1} C_i + \left[C_0^{'} \right] \right) = V_{OUT} \left(\sum_{i=0}^{n-1} \frac{C}{2^{n-i}} + \left[\frac{C}{2^n} \right] \right) = V_{OUT} C$$

$$Q_{SET} = Q_{RDIS}$$

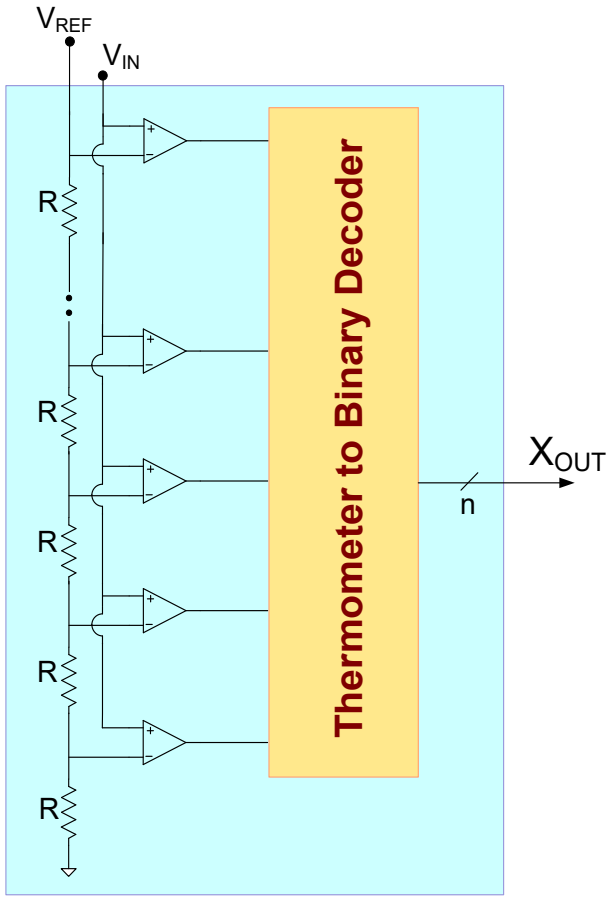
$$V_{REF} \sum_{i=0}^{n-1} d_i \frac{C}{2^{n-i}} = V_{OUT} C$$

$$V_{OUT} = V_{REF} \sum_{i=0}^{n-1} \frac{d_i}{2^{n-i}}$$



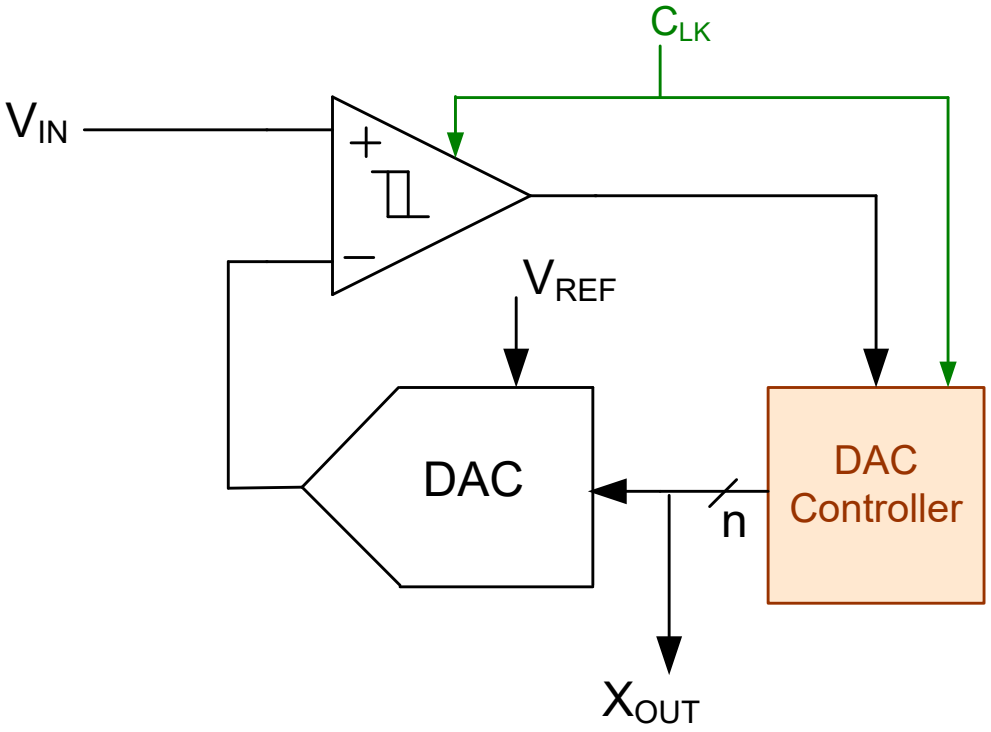
Data Converter Architectures

Flash

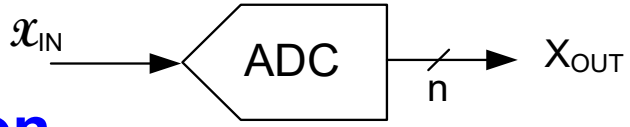


Data Converter Architectures

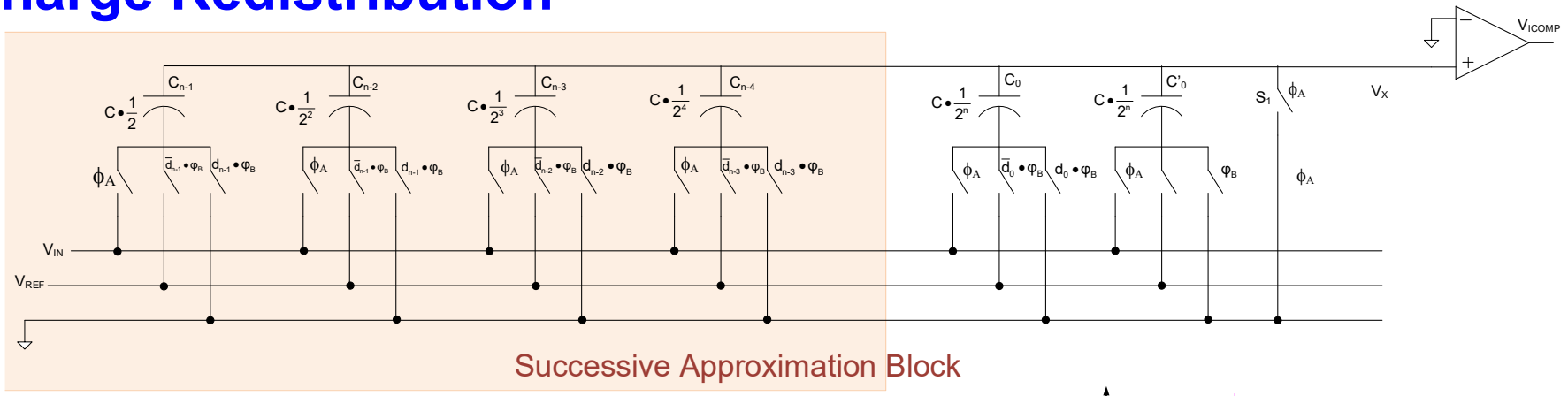
Successive Approximation Register (SAR)



Data Converter Architectures



Charge Redistribution



Redistribute charge with switches to drive Vx to 0

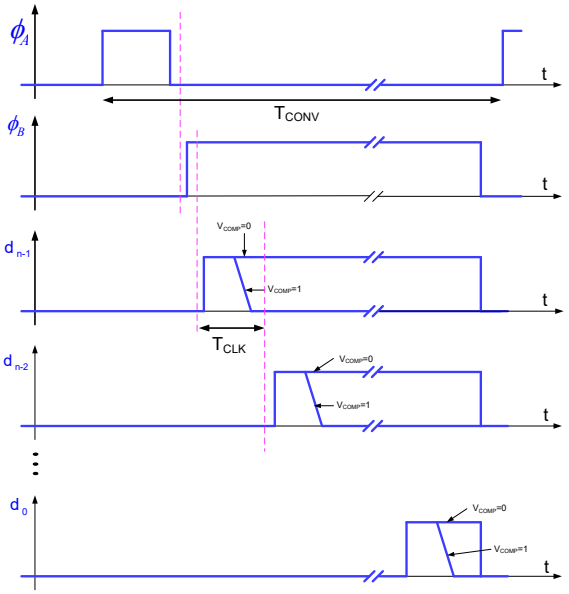
$$Q_{SAM} = V_{IN}\left(\sum_{i=0}^{n-1} C_i + \left[C_0^{'}\right]\right) = V_{IN}\left(\sum_{i=0}^{n-1} \frac{C}{2^{n-i}} + \left[\frac{C}{2^n}\right]\right) = V_{IN}C$$

$$Q_{REDIS} = V_{REF}\sum_{i=0}^{n-1} d_i \frac{C}{2^{n-i}}$$

$$Q_{SAM} = Q_{REDIS}$$

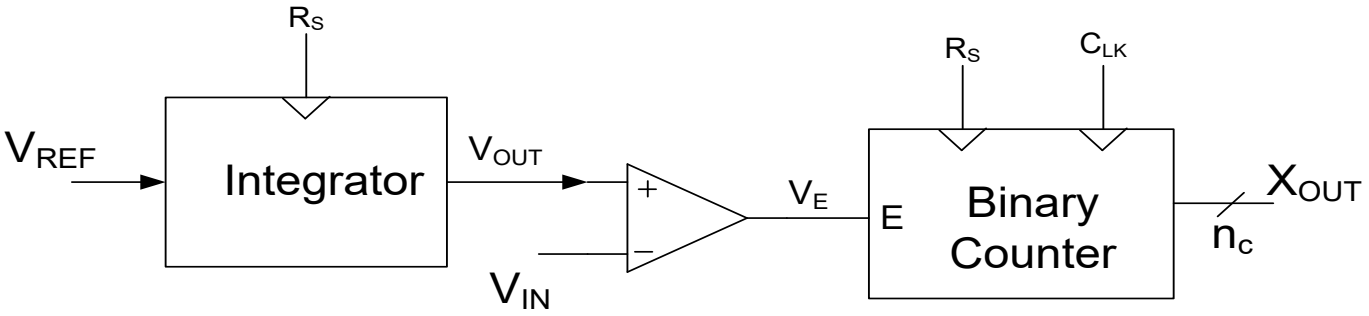
$$V_{REF}\sum_{i=0}^{n-1} d_i \frac{C}{2^{n-i}} = V_{IN}C$$

$$V_{IN} = V_{REF}\sum_{i=0}^{n-1} \frac{d_i}{2^{n-i}}$$



Data Converter Architectures

Single Slope



Comparator Changes States when $V_{IN} = I_0 \int_0^{t_{TR}} V_{REF}\,dt = I_0 t_{TR} V_{REF}$

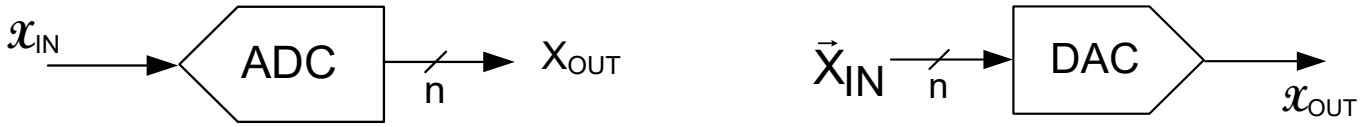
Counter stops when $V_{IN} = t_{TR} V_{REF} I_0 \cong n_{COUNT} T_{CLK} V_{REF} I_0$ → $n_{COUNT} \cong \frac{V_{IN}}{V_{REF}} \bullet \left(\frac{f_{CLK}}{I_0} \right)$

If calibrate so that $2^n \cong \left(\frac{f_{CLK}}{I_0} \right)$ $n_{COUNT} \cong \frac{V_{IN}}{V_{REF}} \bullet 2^n$ ⟷ $V_{IN} \cong \frac{n_{COUNT}}{2^n} \bullet V_{REF}$

Data Converter Architectures

- Many more data converter architectures have been proposed
- Many are some variant of those listed above
- Recall: All typically are perfect if components are ideal
- The major nonideal effects are usually due to one of four issues:
  - Matching performance is not acceptable
  - Speed is limited by parasitics
  - Nonlinearities degrade performance
  - Noise is excessive
- Most data converter design involves sequentially identifying dominant nonideal effect and developing ways to lower it
- Important to observe methods for mitigating nonideal effects as they are often used repeatedly

Performance Characterization of Data Converters



- A very large number of parameters (2^n) characterize the static performance of an ADC!
- And even more parameters needed to characterize the dynamic performance of an ADC
- A large (but much smaller) number of parameters are invariably used to characterize a data converter
- Performance parameters of interest depend strongly on the application
- Very small number of parameters of interest in many/most applications
- "Catalog" data converters are generally intended to satisfy a wide range of applications and thus have much more stringent requirements placed on their performance
- Custom application-specific data converter will generally perform much better than a "catalog" part in the same application

What DAC Architectures are Actually Used?

Listing from Texas Instruments March 1 2023

String	168
R-2R	79
Current Source	52
MDAC	23
Current Sink	17
SAR	9
Pipeline	7
Delta Sigma	4
1-Steering	3
Current Steering	2

A/D Converters

What types are really used?

Consider catalog parts from one vendor – Analog Devices

Flash	2
SAR	233
Pipelined	242
Sigma-Delta	81
Total	559

What do ADCs cost?

A/D Converters

Maximize Filters | Sort by Newest | Choose Parameters | Reset Table | Download to Excel | Help

Part #	Hardware	ADC Resolution (bits)	ADC Output Sample Rate	ADC Channels	Device Architecture	US Price 1000 to 4999 ($ US)	INL in LSB (typ) (LSBs)	Vin Range (typ) (V p-p)	ADC SNR in dBFS (typ) (dBFS)	Power Dissipation (typ) (W)
	0 Values...	16 Values...	16.6 - 2.5G	13 Value...	7 Values S...	0.95 - 916.5	0.1 - 33.55	0.078 - 40	47 - 107.8	21u - 4.2
AD7492-5		12	1.25M	-	SAR	**	-	-	-	16.5m
AD7170		12	125	1	Sigma-Delta	$0.95	-	-	-	150µ
AD7478	-	8	1M	1	SAR	$0.96	-	5.25	-	17.5m
AD7478A	-	8	1.2M	1	SAR	$1.12	-	5.25	-	17.5m
AD7171		16	125	1	Sigma-Delta	$1.15	-	-	-	150µ
AD7999	-	8	140k	4	SAR	$1.35	-	5.5	-	4.7m
AD7468		8	320k	1	SAR	$1.35	-	3.6	-	570µ
AD7091		12	1M	1	SAR	$1.60	-	5.25	-	2.4m
AD7904		8	1M	4	SAR	$1.68	-	5.1	-	13.5m
AD7910		10	250k	1	SAR	$1.77	-	5.25	-	15m
AD7995		10	140k	4	SAR	$1.80	-	5.5	-	4.4m
AD7276		12	3M	1	SAR	$1.85	-	3.6	-	19.8m
AD7908	-	8	1M	8	SAR	$1.87	-	5.05	-	13.5m

What do ADCs cost?

A/D Converters

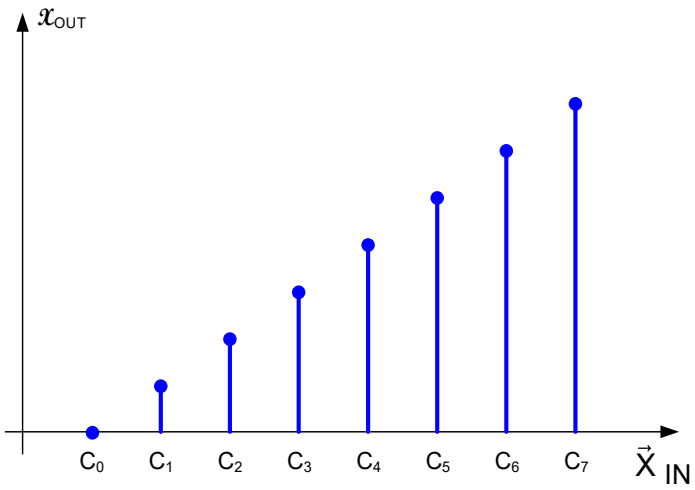
Maximize Filters | Sort by Newest | Choose Parameters | Reset Table | Download to Excel | Help

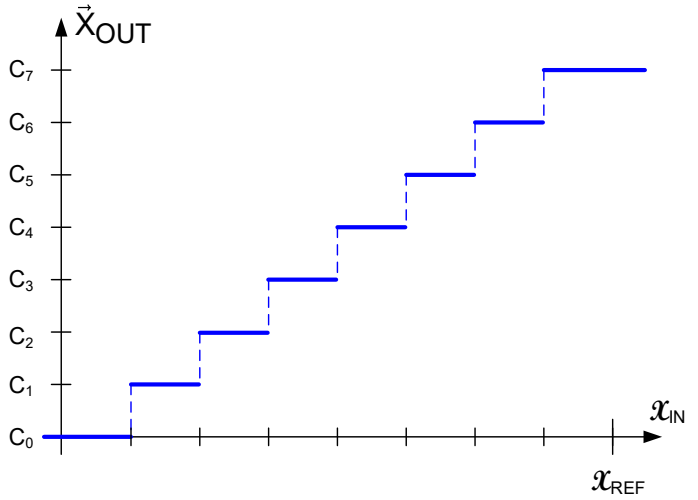
Part #	Hardware	ADC Resolution (bits)	ADC Output Sample Rate	ADC Channels	Device Architecture	US Price 1000 to 4999 ($ US)	INL in LSB (typ) (LSBs)	Vin Range (typ) (V p-p)	ADC SNR in dBFS (typ) (dBFS)	Power Dissipation (typ) (W)
	0 Values...	16 Values...	16.6 - 2.5G	13 Value...	7 Values S...	0.95 - 916.5	0.1 - 33.55	0.078 - 40	47 - 107.8	21u - 4.2
AD10465		14	65M	2	Pipelined	$916.53	-	4	-	3.5
ad9625-2600		12	-	1	Pipelined	$837.42	1	1.1	58.1	4
ad9625-2500		12	2.5G	1	Pipelined	$735.00	1	1.1	58.3	3.9
AD9691	-	14	1250M	2	Pipelined	$692.75	2.6	1.58	63.4	3.8
AD9680-1250		14	1.25G	2	Pipelined	$692.75	3	1.58	63.6	3.7
ad9625-2000		12	2G	1	Pipelined	$624.75	0.9	1.1	59.5	3.48
AD9680-1000		14	1G	2	Pipelined	$584.38	2.5	1.7	67.2	3.3
AD9694		14	500M	4	Pipelined	$488.75	1	-	67.1	1.66

Resolution?

3 bits to 24 bits (one at 32 bits)

Real Simple Concepts





$$x_{OUT} = X_{REF} \sum_{j=1}^{n} \frac{b_{n-j}}{2^j}$$

$$x_{REF} \sum_{j=1}^{n} \frac{d_{n-j}}{2^j} = x_{IN} + \varepsilon$$

- Characterizing performance is a tedious task
- Users must be aware of the “quirks” inherent in data converters
- Designers must understand performance requirements

TEXAS INSTRUMENTS

ADS9120
SBAS710A – SEPTEMBER 2016 – REVISED JUNE 2017

ADS9120 16-Bit, 2.5-MSPS, 15.5-mW, SAR ADC With Enhanced Performance Features

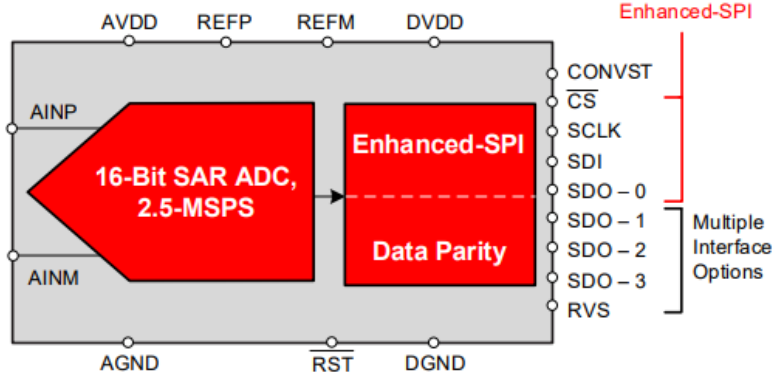
QTY	UNIT PRICE
1	$20.48000
10	$18.82100
25	$18.04120
100	$15.11560

1 Features

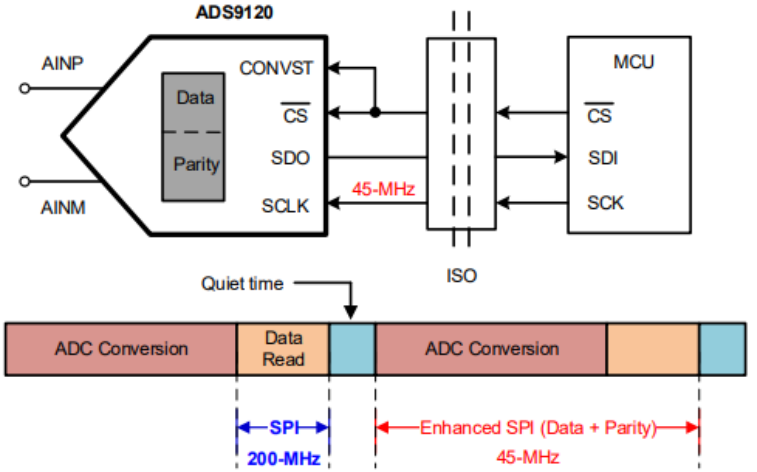
- Sample Rate: 2.5 MSPS
- No Latency Output
- Excellent DC and AC Performance:
  - INL: ±0.25 LSB
  - DNL: ±0.6 LSB
  - SNR: 96 dB, THD: –118 dB
- Wide Input Range:
  - Unipolar Differential Input Range: $\pm V_{REF}$
  - V_{REF} Input Range: 2.5 V to 5 V, Independent of AVDD
- Low-Power Dissipation:
  - 9 mW at 2.5 MSPS (AVDD Only)
  - 15.5 mW at 2.5 MSPS (Total)
  - Flexible Low-Power Modes Enable Power Scaling with Throughput
- Enhanced-SPI (multiSPI™) Digital Interface
- JESD8-7A-Compliant Digital I/O at 1.8-V DVDD
- Fully-Specified Over Extended Temperature Range: –40°C to +125°C
- Small Footprint: 4-mm × 4-mm VQFN

Ease of System Design with ADS9120

ADS9120 Block Diagram



Lowest Clock Speeds at 2.5-MSPS using 3-Wire Enhanced-SPI



6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
AVDD	Analog supply voltage		1.8		V
DVDD	Digital supply voltage		1.8		V
REFP	Positive reference		5		V

6.5 Electrical Characteristics

All specifications are for AVDD = 1.8 V, DVDD = 1.8 V, V_{REF} = 5 V, and f_{DATA} = 2.5 MSPS, unless otherwise noted.
All minimum and maximum specifications are for T_A = –40°C to +85°C, unless otherwise noted.
All typical values are at T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
FSR	Full-scale input range (AINP – AINM)(1)		$-V_{REF}$		V_{REF}	V
V_{IN}	Absolute input voltage (AINP and AINM to REFGND)		–0.1		V_{REF} + 0.1	V
V_{CM}	Common-mode voltage range (AINP + AINM) / 2		(V_{REF} / 2) – 0.1	V_{REF} / 2	(V_{REF} / 2) + 0.1	V
C_{IN}	Input capacitance	In sample mode		60		pF
		In hold mode		4		
I_{IL}	Input leakage current			±1		µA
VOLTAGE REFERENCE INPUT						
V_{REF}	Reference input voltage range		2.5		5	V
I_{REF}	Reference input current	Average current, V_{REF} = 5 V, 2-kHz, full-scale input, throughput = 2.5 MSPS		1.3		mA
DC ACCURACY						
	Resolution			16		Bits
NMC	No missing codes		16			Bits
INL	Integral nonlinearity	T_A = –40°C to +85°C	–0.6	±0.25(2)	0.6	LSB(3)
		T_A = –40°C to +125°C	–0.7	±0.25(2)	0.7	
DNL	Differential nonlinearity	T_A = –40°C to +85°C	–0.6	±0.25(2)	0.6	LSB
		T_A = –40°C to +125°C	–0.7	±0.25	0.7	
$E_{(IO)}$	Input offset error		–1	±0.025(2)	1	mV
dV_{OS}/dT	Input offset thermal drift			1		µV/°C
G_E	Gain error		–0.02	±0.01(2)	0.02	%FS
G_E/dT	Gain error thermal drift			0.25		ppm/°C
	Transition noise			0.35		LSB
CMRR	Common-mode rejection ratio	At dc to 20 kHz		80		dB

Electrical Characteristics (continued)

All specifications are for AVDD = 1.8 V, DVDD = 1.8 V, V_{REF} = 5 V, and f_{DATA} = 2.5 MSPS, unless otherwise noted.
All minimum and maximum specifications are for T_A = –40°C to +85°C, unless otherwise noted.
All typical values are at T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC ACCURACY[4]						
SINAD	Signal-to-noise + distortion	f_{IN} = 2 kHz	94.4	96		dB
		f_{IN} = 100 kHz		95		
		f_{IN} = 500 kHz		83.9		
SNR	Signal-to-noise ratio	f_{IN} = 2 kHz	94.5	96		dB
		f_{IN} = 100 kHz		95.9		
		f_{IN} = 500 kHz		84		
THD	Total harmonic distortion[5]	f_{IN} = 2 kHz		–118		dB
		f_{IN} = 100 kHz		–102		
		f_{IN} = 500 kHz		–101		
SFDR	Spurious-free dynamic range	f_{IN} = 2 kHz		120		dB
		f_{IN} = 100 kHz		108		
		f_{IN} = 500 kHz		106		
DIGITAL INPUTS[6]						
V_{IH}	High-level input voltage		0.65 DVDD		DVDD + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.35 DVDD	V
DIGITAL OUTPUTS[6]						
V_{OH}	High-level output voltage	I_{OH} = 2-mA source	DVDD – 0.45			V
V_{OL}	Low-level output voltage	I_{OH} = 2-mA sink			0.45	V
POWER SUPPLY						
AVDD	Analog supply voltage		1.65	1.8	1.95	V
DVDD	Digital supply voltage		1.65	1.8	1.95	V
IDD	AVDD supply current (AVDD = 1.8 V)	Active, 2.5-MSPS throughput, T_A = –40°C to +85°C		5	6.5	mA
		Active, 2.5-MSPS throughput, T_A = –40°C to +125°C		5	6.75	
		Static, ACQ state		3.7		mA
		Low-power, NAP mode		500		µA
		Power-down, PD state		1		
P_D	AVDD power dissipation (AVDD = 1.8 V)	Active, 2.5-MSPS throughput, T_A = –40°C to +85°C		9	11.7	mW
		Active, 2.5-MSPS throughput, T_A = –40°C to +125°C		9	12.15	
		Static, ACQ state		6.6		mW
		Low-power, NAP mode		900		µW
		Power-down, PD state		1.8		
TEMPERATURE RANGE						
T_A	Operating free-air temperature		–40		125	°C

6.6 Timing Requirements: Conversion Cycle

All specifications are for AVDD = 1.8 V, DVDD = 1.8 V, V_{REF} = 5 V, and f_{DATA} = 2.5 MSPS, unless otherwise noted.
All minimum and maximum specifications are for T_A = –40°C to +85°C. All typical values are at T_A = 25°C. See Figure 1.

		MIN	TYP	MAX	UNIT
TIMING REQUIREMENTS					
f_{cycle}	Sampling frequency			2.5	MHz
t_{cycle}	ADC cycle time period	400			ns
t_{wh_CONVST}	Pulse duration: CONVST high	30			ns
t_{wl_CONVST}	Pulse duration: CONVST low	30			ns
t_{acq}	Acquisition time	100			ns
t_{qt_acq}	Quiet acquisition time(1)	25			ns
t_{d_cnvcap}	Quiet aperture time(1)	10			ns
TIMING SPECIFICATIONS					
t_{conv}	Conversion time	270		290	ns

(1) See Figure 47.

6.7 Timing Requirements: Asynchronous Reset, NAP, and PD

All specifications are for AVDD = 1.8 V, DVDD = 1.8 V, V_{REF} = 5 V, and f_{DATA} = 2.5 MSPS, unless otherwise noted.
All minimum and maximum specifications are for T_A = –40°C to +85°C. All typical values are at T_A = 25°C. See Figure 2 and Figure 3.

		MIN	TYP	MAX	UNIT
TIMING REQUIREMENTS					
t_{wl_RST}	Pulse duration: $\overline{RST}$ low	100			ns
TIMING SPECIFICATIONS					
t_{d_rst}	Delay time: $\overline{RST}$ rising to RVS rising			1250	µs
t_{nap_wkup}	Wake-up time: NAP mode			300	ns
t_{PWRUP}	Power-up time: PD mode			250	µs

6.8 Timing Requirements: SPI-Compatible Serial Interface

All specifications are for AVDD = 1.8 V, DVDD = 1.8 V, V_{REF} = 5 V, and f_{DATA} = 2.5 MSPS, unless otherwise noted.
All minimum and maximum specifications are for T_A = –40°C to +85°C. All typical values are at T_A = 25°C. See Figure 4.

			MIN	TYP	MAX	UNIT
TIMING REQUIREMENTS						
f_{CLK}	Serial clock frequency				75	MHz
t_{CLK}	Serial clock time period		13.33			ns
t_{ph_CK}	SCLK high time		0.45		0.55	t_{CLK}
t_{pl_CK}	SCLK low time		0.45		0.55	t_{CLK}
t_{su_CSCK}	Setup time: $\overline{CS}$ falling to the first SCLK capture edge		5			ns
t_{su_CKDI}	Setup time: SDI data valid to the SCLK capture edge		1.2			ns
t_{ht_CKDI}	Hold time: SCLK capture edge to (previous) data valid on SDI		0.65			ns
t_{ht_CKCS}	Delay time: last SCLK falling to $\overline{CS}$ rising		5			ns
TIMING SPECIFICATIONS						
t_{den_CSDO}	Delay time: $\overline{CS}$ falling to data enable				4.5	ns
t_{dz_CSDO}	Delay time: $\overline{CS}$ rising to SDO going to 3-state				10	ns
t_{d_CKDO}	Delay time: SCLK launch edge to (next) data valid on SDO				6.5	ns
$t_{d\_CSRDY\_f}$	Delay time: $\overline{CS}$ falling to RVS falling				5	ns
$t_{d\_CSRDY\_r}$	Delay time: $\overline{CS}$ rising to RVS rising	After NOP operation			10	ns
		After WR or RD operation			70	

ANALOG DEVICES

4-Channel, 200 kSPS 12-Bit ADC with Sequencer in 16-Lead TSSOP

Data Sheet $2.58 in 1000's **AD7923**

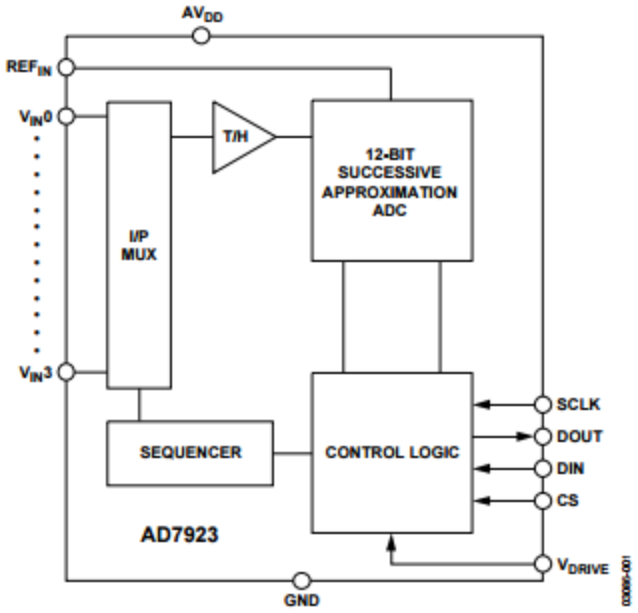
FEATURES

- Fast throughput rate: 200 kSPS
- Specified for AV_{DD} of 2.7 V to 5.25 V
- Low power
  - 3.6 mW max at 200 kSPS with 3 V supply
  - 7.5 mW max at 200 kSPS with 5 V supply
- 4 (single-ended) inputs with sequencer
- Wide input bandwidth
  - 70 dB Min SNR at 50 kHz input frequency
- Flexible power/serial clock speed management
- No pipeline delays
- High speed serial interface SPI®-/QSPI™-/ MICROWIRE™-/DSP-compatible
- Shutdown mode: 0.5 µA max
- 16-lead TSSOP package
- Qualified for automotive applications

GENERAL DESCRIPTION

The AD7923 is a 12-bit, high speed, low power, 4-channel, suc-

FUNCTIONAL BLOCK DIAGRAM



SPECIFICATIONS

AV_{DD} = V_{DRIVE} = 2.7 V to 5.25 V, REF_{IN} = 2.5 V, f_{SCLK} = 20 MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

Parameter	B Version[1]	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE			f_{IN} = 50 kHz sine wave, f_{SCLK} = 20 MHz
Signal-to-(Noise + Distortion) (SINAD)[2]	70	dB min	@ 5 V, −40°C to +85°C
	69	dB min	@ 5 V, 85°C to 125°C, typ 70 dB
	69	dB min	@ 3 V typ 70 dB, −40°C to +125°C
Signal-to-Noise (SNR)[2]	70	dB min	
Total Harmonic Distortion (THD)[2]	−77	dB max	@ 5 V typ, −84 dB
	−73	dB max	@ 3 V typ,−77 dB
Peak Harmonic or Spurious Noise	−78	dB max	@ 5 V typ, −86 dB
(SFDR)[2]	−76	dB max	@ 3 V typ, −80 dB
Intermodulation Distortion (IMD)[2]			f_A = 40.1 kHz, f_B = 41.5 kHz
Second Order Terms	−90	dB typ	
Third Order Terms	−90	dB typ	
Aperture Delay	10	ns typ	
Aperture Jitter	50	ps typ	
Channel-to-Channel Isolation	−85	dB typ	f_{IN} = 400 kHz
Full Power Bandwidth	8.2	MHz typ	@ 3 dB
	1.6	MHz typ	@ 0.1 dB
DC ACCURACY[2]			
Resolution	12	Bits	
Integral Nonlinearity	±1	LSB max	
Differential Nonlinearity	−0.9/+1.5	LSB max	Guaranteed no missed codes to 12 bits
0 V to REF_{IN} Input Range			Straight binary output coding
Offset Error	±8	LSB max	Typ ±0.5 LSB
Offset Error Match	±0.5	LSB max	
Gain Error	±1.5	LSB max	
Gain Error Match	±0.5	LSB max	
0 V to 2 × REF_{IN} Input Range			−REF_{IN} to +REF_{IN} biased about REF_{IN} with twos complement output coding
Positive Gain Error	±1.5	LSB max	
Positive Gain Error Match	±0.5	LSB max	
Zero-Code Error	±8	LSB max	Typ ±0.8 LSB
Zero-Code Error Match	±0.5	LSB max	
Negative Gain Error	±1	LSB max	
Negative Gain Error Match	±0.5	LSB max	
ANALOG INPUT			
Input Voltage Range	0 to REF_{IN}	V	Range bit set to 1
	0 to 2 × REF_{IN}	V	Range bit set to 0, AV_{DD} = 4.75 V to 5.25 V
DC Leakage Current	±1	µA max	
Input Capacitance	20	pF typ	
REFERENCE INPUT			
REF_{IN} Input Voltage	2.5	V	±1% specified performance
DC Leakage Current	±1	µA max	
REF_{IN} Input Impedance	36	kΩ typ	f_{SAMPLE} = 200 kSPS
LOGIC INPUTS			
Input High Voltage, V_{INH}	0.7 × V_{DRIVE}	V min	
Input Low Voltage, V_{INL}	0.3 × V_{DRIVE}	V max	
Input Current, I_{IN}	±1	µA max	Typ 10 nA, V_{IN} = 0 V or V_{DRIVE}
Input Capacitance, C_{IN}[3]	10	pF max	

ANALOG DEVICES

16-Bit, 200 MSPS/250 MSPS Analog-to-Digital Converter

Data Sheet

$120 in 1000's

AD9467

FEATURES

- 75.5 dBFS SNR to 210 MHz at 250 MSPS
- 90 dBFS SFDR to 300 MHz at 250 MSPS
- SFDR at 170 MHz at 250 MSPS
  - 92 dBFS at −1 dBFS
  - 100 dBFS at −2 dBFS
- 60 fs rms jitter
- Excellent linearity at 250 MSPS
  - DNL = ±0.5 LSB typical
  - INL = ±3.5 LSB typical
- 2 V p-p to 2.5 V p-p (default) differential full-scale input (programmable)
- Integrated input buffer
- External reference support option
- Clock duty cycle stabilizer
- Output clock available
- Serial port control
  - Built-in selectable digital test pattern generation
  - Selectable output data format
- LVDS outputs (ANSI-644 compatible)
- 1.8 V and 3.3 V supply operation

APPLICATIONS

- Multicarrier, multimode cellular receivers
- Antenna array positioning
- Power amplifier linearization
- Broadband wireless
- Radar
- Infrared imaging
- Communications instrumentation

FUNCTIONAL BLOCK DIAGRAM

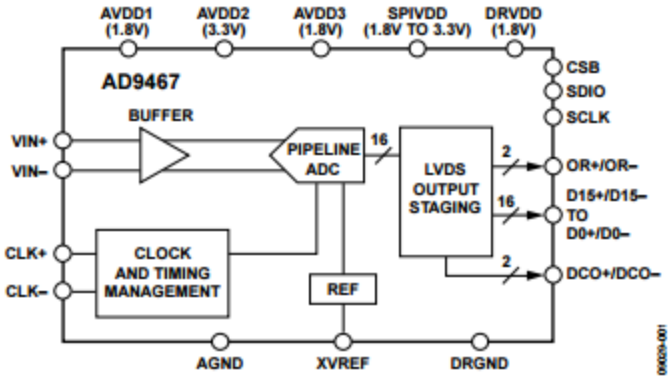


Figure 1.

A data clock output (DCO) for capturing data on the output is provided for signaling a new output bit.

The internal power-down feature supported via the SPI typically consumes less than 5 mW when disabled.

Optional features allow users to implement various selectable operating conditions, including input range, data format select, and output data test patterns.

The AD9467 is available in a Pb-free, 72-lead, LFCSP specified over the −40°C to +85°C industrial temperature range.

SPECIFICATIONS

AVDD1 = 1.8 V, AVDD2 = 3.3 V, AVDD3 = 1.8 V, DRVDD = 1.8 V, specified maximum sampling rate, 2.5 V p-p differential input, 1.25 V internal reference, AIN = −1.0 dBFS, DCS on, default SPI settings, unless otherwise noted.

Table 1.

Parameter[1]	Temp	Min	Typ	Max	Unit
RESOLUTION		16			Bits
ACCURACY					
No Missing Codes	Full		Guaranteed		
Offset Error	Full	−200	0	+200	LSB
Gain Error	Full	−3.9	−0.1	+2.6	%FSR
Differential Nonlinearity (DNL)[2]	Full	−0.9	±0.5	+1.5	LSB
Integral Nonlinearity (INL)[2]	Full	−12	±3.5	+12	LSB
TEMPERATURE DRIFT					
Offset Error	Full		±0.023		%FSR/°C
Gain Error	Full		±0.036		%FSR/°C
ANALOG INPUTS					
Differential Input Voltage Range (Internal VREF = 1 V to 1.25 V)	Full	2	2.5	2.5	V p-p
Common-Mode Voltage	25°C		2.15		V
Differential Input Resistance	25°C		530		Ω
Differential Input Capacitance	25°C		3.5		pF
Full Power Bandwidth	25°C		900		MHz
XVREF INPUT					
Input Voltage	Full	1		1.25	V
Input Capacitance	Full		3		pF
POWER SUPPLY					
AVDD1	Full	1.75	1.8	1.85	V
AVDD2	Full	3.0	3.3	3.6	V
AVDD3	Full	1.7	1.8	1.9	V
DRVDD	Full	1.7	1.8	1.9	V
I_{AVDD1}	Full		567	620	mA
I_{AVDD2}	Full		55	61	mA
I_{AVDD3}	Full		31	35	mA
I_{DRVDD}	Full		40	43	mA
Total Power Dissipation (Including Output Drivers)	Full		1.33	1.5	W
Power-Down Dissipation	Full		4.4	90	mW

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions and how these tests were completed.
[2] Measured with a low input frequency, full-scale sine wave, with approximately 5 pF loading on each output bit.

AC SPECIFICATIONS

AVDD1 = 1.8 V, AVDD2 = 3.3 V, AVDD3 = 1.8 V, DRVDD = 1.8 V, specified maximum sampling rate, 2.5 V p-p differential input, 1.25 V internal reference, AIN = −1.0 dBFS, DCS on, default SPI settings, unless otherwise noted.

Table 2.

Parameter[1]	Temp	Min	Typ	Max	Unit
ANALOG INPUT FULL SCALE		2.5	2/2.5		V p-p
SIGNAL-TO-NOISE RATIO (SNR)					
f_{IN} = 5 MHz	25°C		74.7/76.4		dBFS
f_{IN} = 97 MHz	25°C		74.5/76.1		dBFS
f_{IN} = 140 MHz	25°C		74.4/76.0		dBFS
f_{IN} = 170 MHz	25°C	73.7	74.3/75.8		dBFS
	Full	71.5			dBFS
f_{IN} = 210 MHz	25°C		74.0/75.5		dBFS
f_{IN} = 300 MHz	25°C		73.3/74.6		dBFS
SIGNAL-TO-NOISE AND DISTORTION RATIO (SINAD)					
f_{IN} = 5 MHz	25°C		74.6/76.3		dBFS
f_{IN} = 97 MHz	25°C		74.4/76.0		dBFS
f_{IN} = 140 MHz	25°C		74.4/76.0		dBFS
f_{IN} = 170 MHz	25°C	72.4	74.2/75.8		dBFS
	Full	71.0			dBFS
f_{IN} = 210 MHz	25°C		73.9/75.4		dBFS
f_{IN} = 300 MHz	25°C		73.1/74.4		dBFS
EFFECTIVE NUMBER OF BITS (ENOB)					
f_{IN} = 5 MHz	25°C		12.1/12.4		Bits
f_{IN} = 97 MHz	25°C		12.1/12.3		Bits
f_{IN} = 140 MHz	25°C		12.1/12.3		Bits
f_{IN} = 170 MHz	25°C		12.0/12.3		Bits
	Full	11.5			Bits
f_{IN} = 210 MHz	25°C		12.0/12.2		Bits
f_{IN} = 300 MHz	25°C		11.9/12.1		Bits
SPURIOUS-FREE DYNAMIC RANGE (SFDR) (INCLUDING SECOND AND THIRD HARMONIC DISTORTION)					
f_{IN} = 5 MHz	25°C		98/97		dBFS
f_{IN} = 97 MHz	25°C		95/93		dBFS
f_{IN} = 140 MHz	25°C		94/95		dBFS
f_{IN} = 170 MHz	25°C	82	93/92		dBFS
	Full	82			dBFS
f_{IN} = 210 MHz	25°C		93/92		dBFS
f_{IN} = 300 MHz	25°C		93/90		dBFS
SFDR (INCLUDING SECOND AND THIRD HARMONIC DISTORTION)					
f_{IN} = 5 MHz at −2 dB Full Scale	25°C		100/100		dBFS
f_{IN} = 97 MHz at −2 dB Full Scale	25°C		97/97		dBFS
f_{IN} = 140 MHz at−2 dB Full Scale	25°C		100/95		dBFS
f_{IN} = 170 MHz at −2 dB Full Scale	25°C		100/100		dBFS
f_{IN} = 210 MHz at −2 dB Full Scale	25°C		93/93		dBFS
f_{IN} = 300 MHz at −2 dB Full Scale	25°C		90/90		dBFS
WORST OTHER (EXCLUDING SECOND AND THIRD HARMONIC DISTORTION)					
f_{IN} = 5 MHz	25°C		98/97		dBFS
f_{IN} = 97 MHz	25°C		97/93		dBFS
f_{IN} = 140 MHz	25°C		97/95		dBFS
f_{IN} = 170 MHz	25°C	88	97/93		dBFS
	Full	82			dBFS
f_{IN} = 210 MHz	25°C		97/95		dBFS
f_{IN} = 300 MHz	25°C		97/95		dBFS

SWITCHING SPECIFICATIONS

AVDD1 = 1.8 V, AVDD2 = 3.3 V, AVDD3 = 1.8 V, DRVDD = 1.8 V, specified maximum sampling rate, 2.5 V p-p differential input, 1.25 V internal reference, AIN = −1.0 dBFS, DCS on, default SPI settings, unless otherwise noted.

Table 4.

Parameter[1]	Temp	Min	Typ	Max	Unit
CLOCK[2]					
Clock Rate	Full	50		250	MSPS
Clock Pulse Width High (t_{CH})	Full		2		ns
Clock Pulse Width Low (t_{CL})	Full		2		ns
OUTPUT PARAMETERS[2, 3]					
Propagation Delay (t_{PD})	25°C		3		ns
Rise Time (t_R) (20% to 80%)	25°C		200		ps
Fall Time (t_F) (20% to 80%)	25°C		200		ps
DCO Propagation Delay (t_{CPD})	25°C		3		ns
DCO to Data Delay (t_{SKEW})	Full	−200		+200	ps
Wake-Up Time (Power-Down)	Full		100		ms
Pipeline Latency	Full		16		Clock cycles
APERTURE					
Aperture Delay (t_A)	25°C		1.2		ns
Aperture Uncertainty (Jitter)	25°C		60		fs rms
Out-of-Range Recovery Time	25°C		1		Clock cycles

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions and how these tests were completed.
[2] Can be adjusted via the SPI interface.
[3] Measurements were made using a part soldered to FR-4 material.

Designers must understand performance requirements !

Users must be aware of the “quirks” inherent in data converters !

Performance Characterization of Data Converters

- Static characteristics
  - Resolution
  - Least Significant Bit (LSB)
  - Offset and Gain Errors
  - Absolute Accuracy
  - Relative Accuracy
  - Integral Nonlinearity (INL)
  - Differential Nonlinearity (DNL)
  - Monotonicity (DAC)
  - Missing Codes (ADC)
  - Low-f Spurious Free Dynamic Range (SFDR)
  - Low-f Total Harmonic Distortion (THD)
  - Effective Number of Bits (ENOB)
  - Power Dissipation

Performance Characterization of Data Converters

- Dynamic characteristics
  - Conversion Time or Conversion Rate (ADC)
  - Settling time or Clock Rate (DAC)
  - Sampling Time Uncertainty (aperture uncertainty or aperture jitter)
  - Dynamic Range
  - Spurious Free Dynamic Range (SFDR)
  - Total Harmonic Distortion (THD)
  - Signal to Noise Ratio (SNR)
  - Signal to Noise and Distortion Ratio (SNDR)
  - Sparkle Characteristics
  - Effective Number of Bits (ENOB)

Dynamic characteristics

- Degradation of dynamic performance parameters often due to nonideal effects in time-domain performance

- Dynamic characteristics of high resolution data converters often challenging to measure, to simulate, to understand source of contributions, and to minimize

Example: An n-bit ADC would often require SFDR at the 6n+6 bit level or better. Thus, considering a 14-bit ADC, the SFDR would be expected to be at the -90dB level or better. If the input to the ADC is a 1V p-p sinusoidal waveform, the second harmonic term would need to be at the $10^{(-90dB/20dB)} = 32\mu V$ level. A 32uV level is about 1part in 30,000. Signals at this level are difficult to accurately simulate in the presence of a 1V level signal. For example, convergence parameters in simulators and sample (strobe) points used in data acquisition adversely affect simulation results and observing the time domain waveforms that contribute to nonlinearity at this level and relationships between these waveforms and the sources of nonlinearity is often difficult to visualize. Simulation errors that are at the 20dB level or worse can occur if the simulation environment is not correctly established.

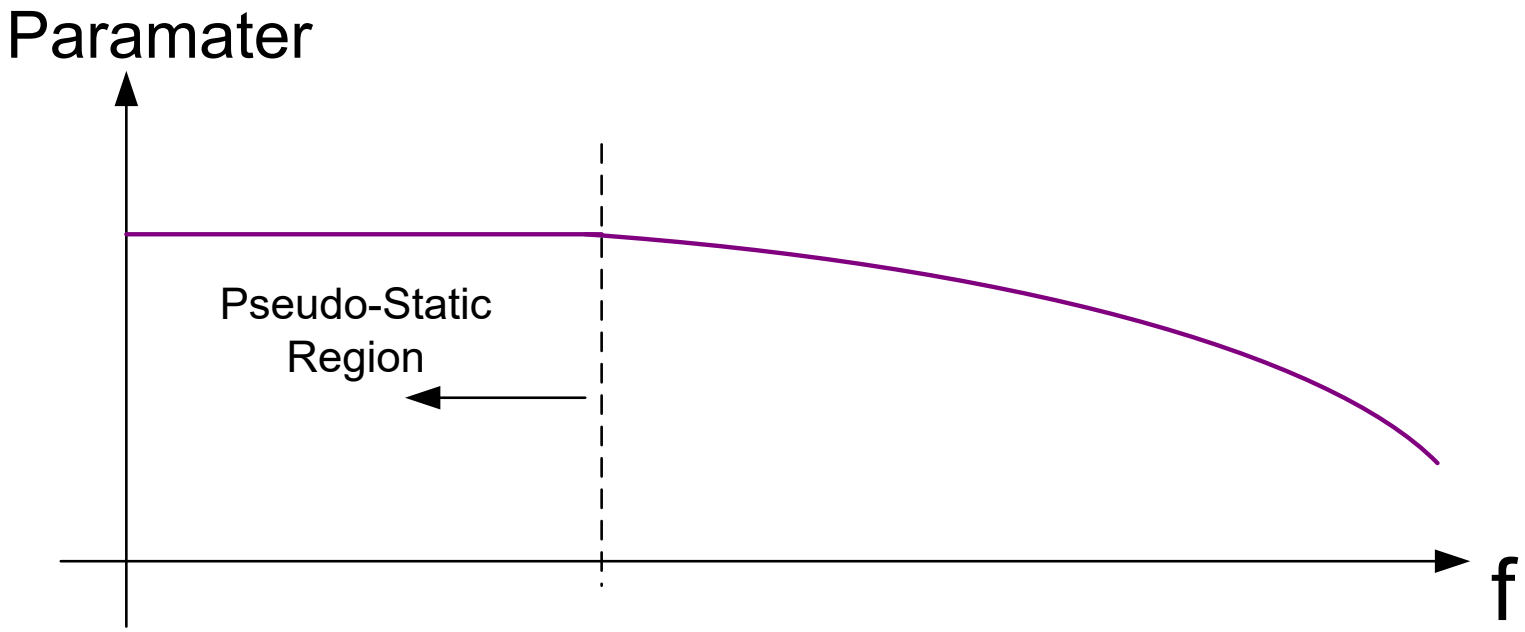
Performance Characterization of Data Converters

What is meant by “low frequency” ?

Operation at frequencies so low that further decreases in frequency cause no further changes in a parameter of interest

Low frequency operation is often termed Pseudo-static operation

Low-frequency or Pseudo-Static Performance



Performance Characterization of Data Converters

- Static characteristics

⇒ Resolution
⇒ Least Significant Bit (LSB)
⇒ Offset and Gain Errors
  – Absolute Accuracy
  – Relative Accuracy
⇒ Integral Nonlinearity (INL)
  – Differential Nonlinearity (DNL)
  – Monotonicity (DAC)
  – Missing Codes (ADC)
  – Low-f Spurious Free Dynamic Range (SFDR)
  – Low-f Total Harmonic Distortion (THD)
  – Effective Number of Bits (ENOB)
  – Power Dissipation

Performance Characterization

Resolution

- Number of distinct analog levels in a DAC
- Number of digital output codes in ADC
- In most cases this is a power of 2
- If a converter can resolve 2^n levels, then we term it an n-bit converter
  - 2^n analog outputs for an n-bit DAC
  - 2^n-1 transition points for an n-bit ADC
- Resolution is often determined by architecture and thus not measured
- Effective resolution can be defined and measured
  - If N_x levels can be resolved for an DAC then

$$n_{EQ} = \frac{\log N_x}{\log 2}$$

  - If N_x-1 transition points in an ADC, then

$$n_{EQ} = \frac{\log N_x}{\log 2}$$

Performance Characterization

Least Significant Bit

Assume $N = 2^n$

Generally Defined by Manufacturer to be

$$x_{LSB} = x_{REF}/N$$

Effective Value of LSB can be Measured

For DAC: x_{LSB} is equal to the maximum increment in the output for a single bit change in the Boolean input

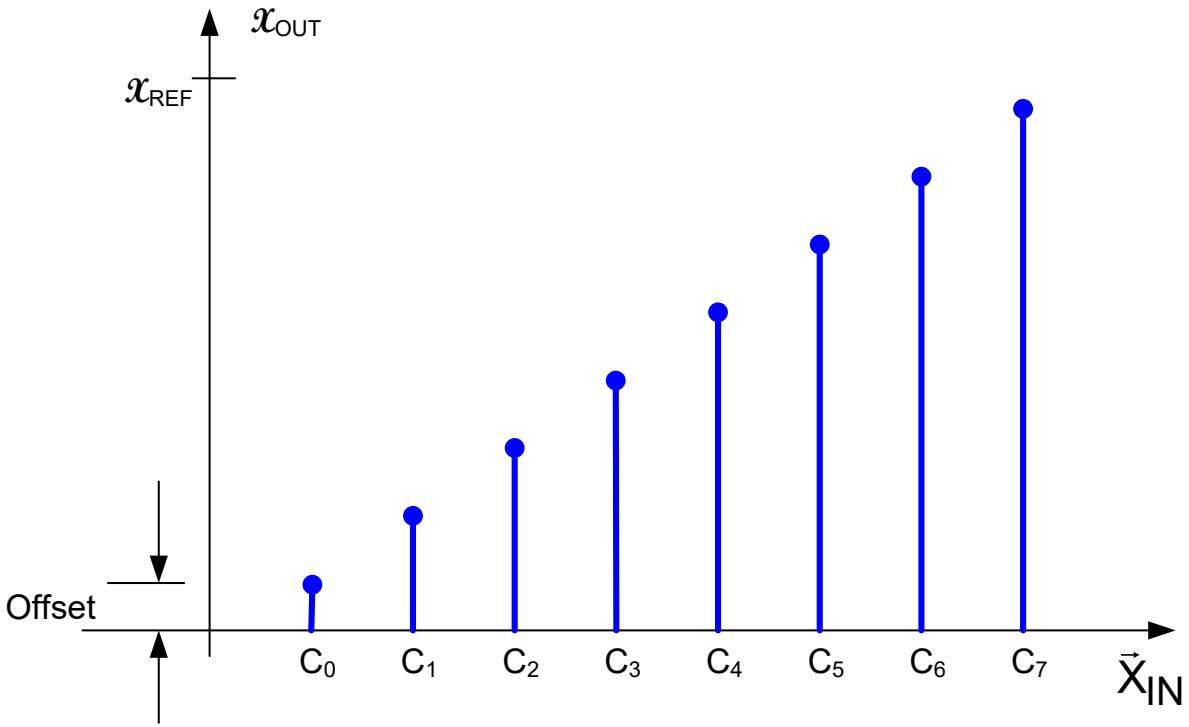
For ADC: x_{LSB} is equal to the maximum distance between two adjacent transition points

Performance Characterization

Offset For DAC the offset is (assuming 0 is ideal value of x_{OUT}(<0,…0>)

x_{OUT} (<0,…, 0>) - absolute

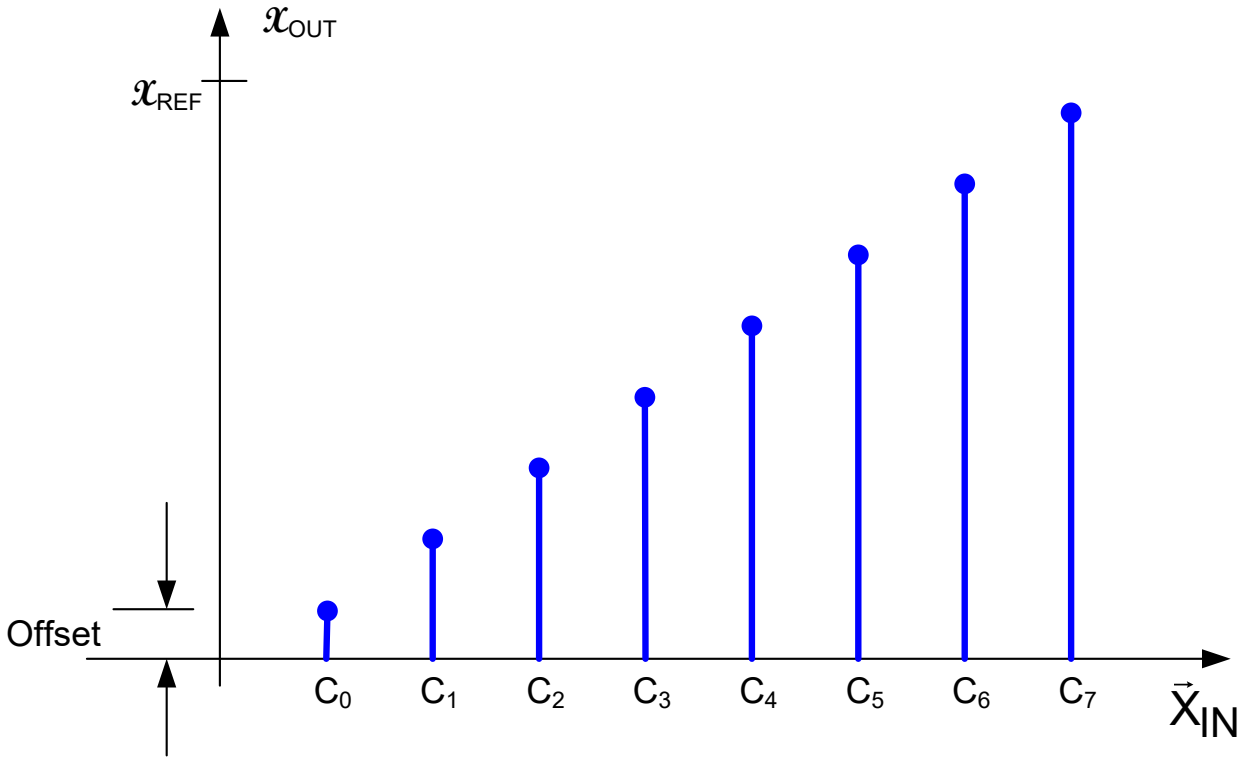
$$\frac{x_{OUT}(\langle 0,...,0\rangle)}{x_{LSB}}$$ - in LSB



(If ideal value of x_{OUT}(<0,…0>) ≠ 0, offset is shift from ideal value at <0,…0>)

Performance Characterization

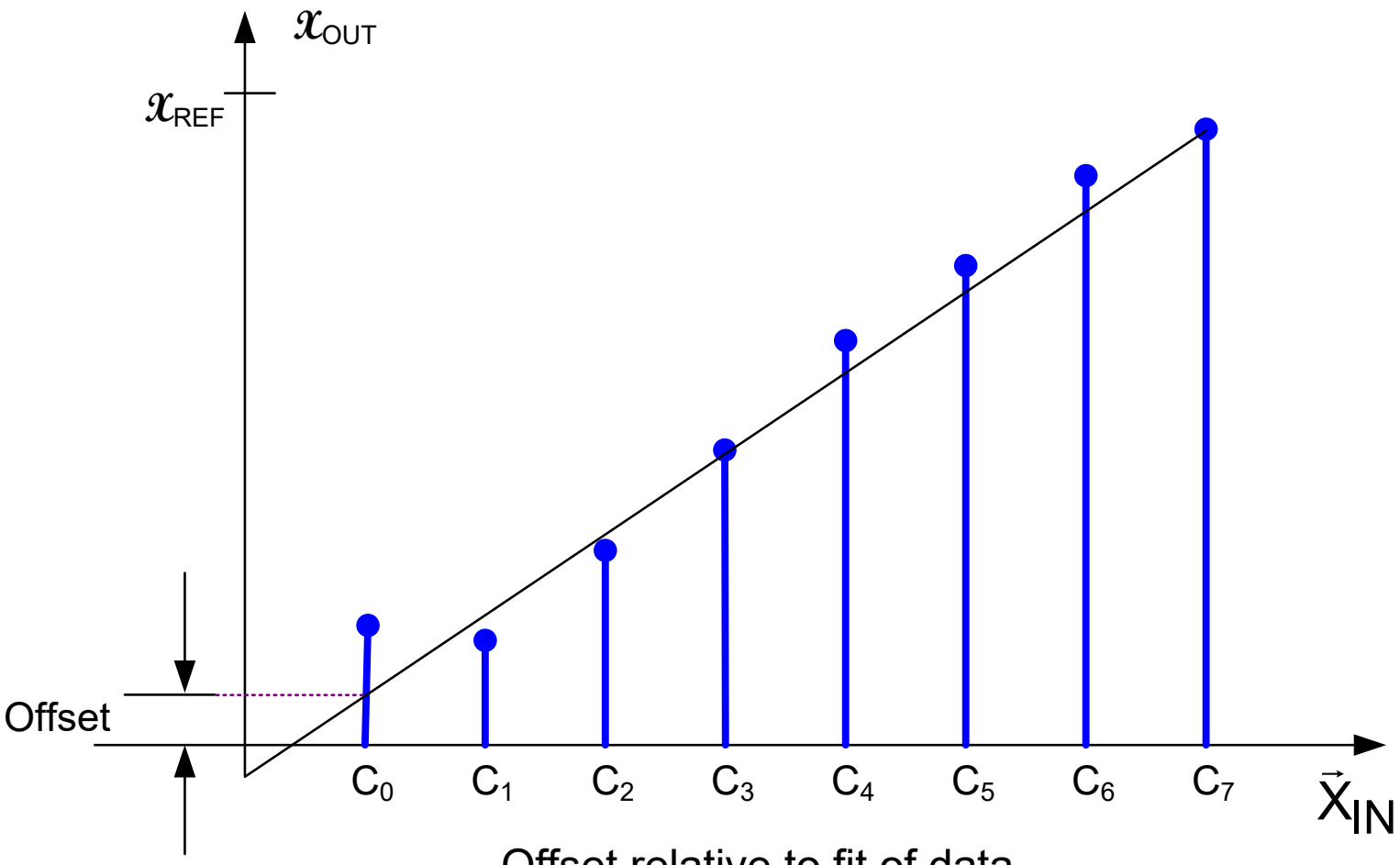
Offset (for DAC)



- Offset strongly (totally) dependent upon performance at a single point
- Probably more useful to define relative to a fit of the data

Performance Characterization

Offset (for DAC)



Offset relative to fit of data

Though usually more useful, not standard (more challenging to test)

Stay Safe and Stay Healthy !

End of Lecture 26